Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A wireless receiver comprising:

a receiver ~~circuit~~ that receives a wireless signal;

a demodulator ~~circuit~~ coupled to the receiver ~~circuit~~, the demodulator ~~circuit~~ recovering a data signal and ~~an first~~ at least one clock signal from ~~the~~ at least one signal output by the receiver circuit;

a computer configured to generate a read signal; and

a first-in first-out memory ~~(FIFO)~~ coupled to the demodulator ~~circuit~~ to receive the data signal and the ~~first~~ at least one clock signal, wherein the ~~FIFO~~ first-in first-out memory stores the data signal in ~~synchronization with~~ response to the ~~first~~ at least one clock signal, and wherein the first-in first-out memory is coupled to the computer to receive the read signal.

2. (New) The wireless receiver of claim 1 wherein the read signal is synchronized with a computer clock signal.

3. (New) The wireless receiver of claim 1 wherein the computer reads the data signal from the first-in first-out memory without synchronizing a clock to the at least one clock signal.

4. (New) The wireless receiver of claim 1 wherein the computer operates at a higher speed than the at least one clock signal.

5. (New) The wireless receiver of claim 5 wherein the computer reads the data signal from the first-in first-out memory in bursts.

6. (New) The wireless receiver of claim 1 wherein the first-in first-out memory is sized in accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

7. (New) The wireless receiver of claim 1 wherein the first-in first-out memory is sized in accordance with a length of data transmitted.

8. (New) The wireless receiver of claim 1 wherein the first-in first-out memory is sized in accordance with a product of a length of data transmitted and a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

9. (New) A wireless receiver comprising:

a receiver that receives a wireless signal;

a demodulator coupled to the receiver, the demodulator recovering a data signal and at least one clock signal from at least one signal output by the receiver circuit;

a first first-in first-out memory coupled to the demodulator to receive the data signal and the at least one clock signal, wherein the first first-in first-out memory stores the data signal in response to the at least one clock signal, and wherein the first first-in first-out memory is coupled to receive a read signal; and

a data processor configured to generate the read signal and coupled to the first first-in first-out memory to receive the data signal, the data processor comprising a second first-in first-out memory for storing the data signal received from the first first-in first-out data memory.

10. (New) The wireless receiver of claim 9 comprising a computer coupled to the data processor to receive the data signal stored in the second first-in first-out memory.

11. (New) The wireless receiver of claim 10 wherein the computer sends a signal to the data processor to receive the data signal stored in the second first-in first-out memory.

12. (New) The wireless receiver of claim 9 wherein the data processor reads the data signal from the first first-in first-out memory in bursts.

13. (New) The wireless receiver of claim 9 wherein the data processor reads the data signal from the first first-in first-out memory at a constant rate.

14. (New) A method for receiving data comprising:

receiving a wireless signal;

recovering a data signal and at least one clock signal from the received wireless signal; and

storing the data signal into a first-in first-out memory in response to the at least one clock signal; and

providing, by a computer, a read signal to the first-in first-out memory.

15. (New) The method of claim 14 wherein the read signal is synchronized with a computer clock signal.

16. (New) The method of claim 14 wherein the computer reads the data signal from the first-in first-out memory without synchronizing a clock to the at least one clock signal.

17. (New) The method of claim 14 wherein the computer operates at a higher speed than the at least one clock signal.

18. (New) The method of claim 14 wherein the computer reads the data signal from the first-in first-out memory in bursts.

19. (New) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

20. (New) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a length of data transmitted.

21. (New) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a product of a length of data transmitted and a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

22. (New) A method for receiving data comprising:

receiving a wireless signal;

recovering a data signal and at least one clock signal from the received wireless signal; and

storing the data signal into a first first-in first-out memory in response to the at least one clock signal;

providing a read signal to the first first-in first-out memory to read the data signal out of the first first-in first-out memory; and

storing the data signal read out of the first first-in first-out memory into a second first-in first-out memory.

23. (New) The method of claim 22 wherein the second first-in first-out memory resides in a data processor.

24. (New) The method of claim 23 comprising providing the data signal stored in the second first-in first-out memory to a computer.

25. (New) The method of claim 24 wherein the computer sends a signal to the data processor to receive the data signal stored in the second first-in first-out memory.

26. (New) The method of claim 22 comprising reading the data signal from the first first-in first-out memory in bursts.

27. (New) The method of claim 22 comprising reading the data signal from the first first-in first-out memory at a constant rate.